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<b>Notice of Allowability</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/627,855	KIM, MIN-SU	
	<b>Examiner</b>	<b>Art Unit</b>	
	Cassandra Cox	2816	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**  
 All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 4/15/05.
2. ☒ The allowed claim(s) is/are 1-16,21,22,27-42,46-48 and 52-62.
3. ☒ The drawings filed on 25 July 2003 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☒ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☒ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
  - \* Certified copies not received: \_\_\_\_\_.

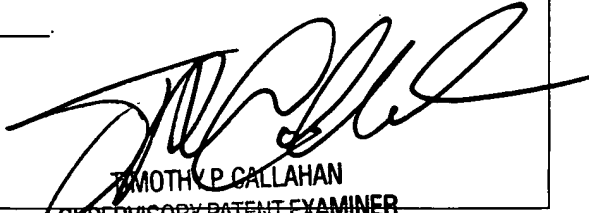
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
  - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
    - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
  - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |   |   |
|---|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892)  | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)           |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                | 6. <input type="checkbox"/> Interview Summary (PTO-413),<br>Paper No./Mail Date _____ |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),<br>Paper No./Mail Date _____ | 7. <input type="checkbox"/> Examiner's Amendment/Comment                              |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br>of Biological Material          | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance  |
|   | 9. <input type="checkbox"/> Other _____   |

  
 TIMOTHY P. CALLAHAN  
 SUPERVISORY PATENT EXAMINER  
 TECHNOLOGY CENTER 2800  
 Date 20050430

## DETAILED ACTION

### *Allowable Subject Matter*

1. Claims 1-16, 21-22, 27-42, 46-48, and 52-62 are allowed.
2. The following is an examiner's statement of reasons for allowance: Claims 1-14 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 1 wherein the sense amplifier comprises a first controller (15) which is connected to the first sense-amplifying unit (11) and sets the output signal (O1) in response to a reset signal (RESET) and an inverted signal (/RESET) of the reset signal; a second controller (17) which is connected to the second sense-amplifying unit (13) and resets the complementary signal (O2) of the output signal in response to the reset signal (RESET) and the inverted signal (/RESET) of the reset signal; and a current source (19) which is connected to the first sense-amplifying unit (11), the second sense-amplifying unit (13), the first controller (15), and the second controller (17) and responds to the clock signal in combination with the rest of the limitations of the base claims and any intervening claims. Claims 27-40 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the sense amplifier comprises a first controller (35) which is connected to the first sense-amplifying unit (31) and sets the output signal (O1) in response to a reset signal (RESET) and an inverted signal (/RESET) of the reset signal; and a second controller (37) which is connected to the second sense-amplifying unit (33) and resets the complementary signal (O2) of the output signal in response to the reset signal (RESET) and the inverted signal (/RESET) of the reset signal in combination with the rest of the limitations of the base claims and

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any intervening claims. Claims 41-42, 46-48, and 52 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the first sense-amplifying unit (31) comprises a first PMOS transistor (P311); a second PMOS transistor (P312); a third PMOS transistor (P313); a first NMOS transistor (N311); a second NMOS transistor (N312); and a third NMOS transistor (N313) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 53 and 55 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the second sense-amplifying unit (33) comprises a first PMOS transistor (P331); a second PMOS transistor (P332); a third PMOS transistor (P333); a first NMOS transistor (N331); a second NMOS transistor (N332); and a third NMOS transistor (N333) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 54 and 56 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the controller comprises a first NMOS transistor (N451), a second NMOS transistor (N452), and a third NMOS transistor (N453) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 15-16 and 21-22 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the first sense-amplifying unit (31) comprises a first PMOS transistor (P311); a second PMOS transistor (P312); a third PMOS transistor (P313); a first NMOS transistor (N311); a second NMOS transistor (N312); and a third

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NMOS transistor (N313) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 57 and 60 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the second sense-amplifying unit (33) comprises a first PMOS transistor (P331); a second PMOS transistor (P332); a third PMOS transistor (P333); a first NMOS transistor (N331); a second NMOS transistor (N332); and a third NMOS transistor (N333) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 58 and 61 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the controller comprises a first NMOS transistor (N451), a second NMOS transistor (N452), and a third NMOS transistor (N453) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 59 and 62 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the current source (19) includes an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the first sense-amplifying unit (11), the second sense-amplifying unit (13), and the controller (25), and the clock signal (CLK) is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

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accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC  


April 30, 2005